An Integration Scheme for RF Power Harvesting

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***Abstract*— This paper describes an integration scheme for RF energy harvesting. The scheme includes a resonant voltage boosting network, which provides high amplitude swing from a small signal; and a rectifier that produces DC voltage. Design issues are addressed. Testing circuits are implemented in a Silicon-on-Glass technology. Simulation results show that a DC voltage of 0.8 V can be achieved at -20dBm input energy level at 868.3 MHz ISM band. This would correspond to a potential working distance of 10 meters.**

***Index Terms*— Low-power RF, Passive transponder, Power Harvesting, Radio-frequency identification (RFID), Rectifiers, Unobtrusive radio**

I. INTRODUCTION

Ever since the first successful demonstration of wireless power and data transfer in biomedical systems [1], Radio Frequency Identification (RFID) technology has experienced rapid growth in various applications, such as access control, public transportation, logistics, airline baggage tracking. A simple RFID system includes a reader and a number of transponders (tags). Usually, passive RFID tags work in a shorter range and lower frequency, while longer distance applications are dominated by active tags [2]. Since lower power consumption is one major trend in RF circuit design, a self-powered system by means of energy harvesting becomes very attractive, since it can serve as the enabling technology for novel applications such as ambient intelligence [3].

The RF energy radiated by a centered base station is a robust source to support the passive transponders. A typical RF energy harvesting scheme is shown in Fig. 1. RF power is rectified and stored to provide the DC voltage supply. The scheme of Fig. 1 has been successfully demonstrated in previous research activities [4, 5]. However, the requirement of a relatively high induced RF voltage limits the working range to less than 3 meters.

According to the regulations in Europe, the base station transmit power is limited to 500-mW ERP in the 868MHz ISM band. This means the power available for the operation of the passive transponder is approximately -20dBm at 10 meters distance [2]. In this paper, an attempt is made to address the challenges of implementing an integrated energy harvesting scheme at this power level.

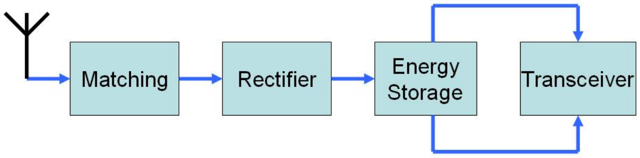

Fig. 1. Block diagram of RF energy harvesting

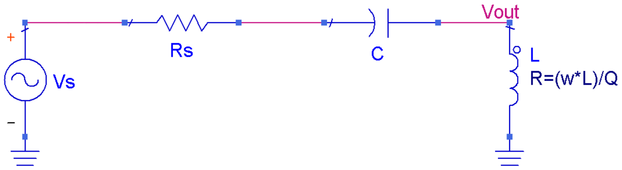

Fig. 2. Simple resonant tank

By employing a resonant-tank based voltage boosting network and performing a careful analysis of the rectifier, we showed that the proposed scheme is a promising solution of energy supply for self-powered radio systems. Simulation results of the test circuit revealed that a DC voltage of 0.8 volts can be achieved from a -20dBm RF signal at 868.3 MHz.

II. ARCHITECTURE

A. Voltage Boosting Network

For a typical 50Ω antenna, the -20dBm received RF signal power means an amplitude of 32mV. The peak voltage of the AC signal is much smaller than the diode threshold. In order to sufficiently drive the rectifier, a voltage boosting network based on resonant tank is employed to produce a larger voltage swing.

Fig. 2 shows a simple serial resonant tank. The amplitude of the voltage at Vout is decided by

$$Vout = Vs \cdot \left| \frac{j\omega L + \dfrac{\omega L}{Q}}{j\omega L + \dfrac{\omega L}{Q} + \dfrac{1}{j\omega C} + Rs} \right| \tag{1}$$

where Q is the quality factor of the inductor. In the ideal case, the highest output voltage is achieved at the resonant frequency

$$f = \frac{1}{2\pi \cdot \sqrt{LC}} \tag{2}$$

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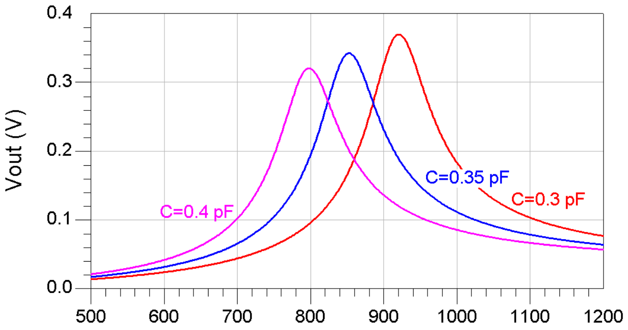

Fig. 3. Output boosted voltage as a function of input signal frequency

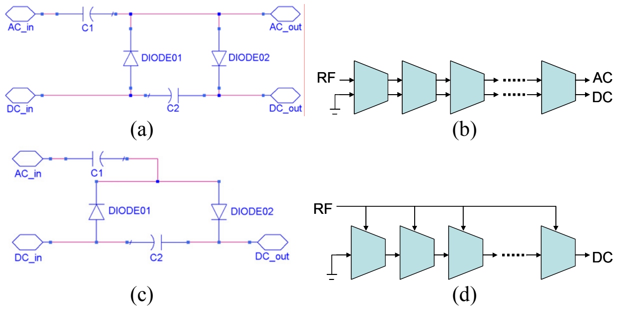

Fig. 4. Single Villard voltage double (a) and cascaded Villard voltage doublers (b); single Dickson voltage multiplier (c) and cascaded Dickson voltage multipliers (d)

and is determined by

$$Vout = \frac{1}{Rs} \cdot \sqrt{\frac{L}{C}} \cdot Vs \qquad (3)$$

According to (3), the square of the boosted voltage amplitude is proportional to the inductance and inversely proportional to the capacitance. The rule of thumb would to make the inductance as large as possible, and choose a suitable capacitance for a given frequency. As shown in Fig. 3, with a fixed inductance, smaller capacitance brings higher output voltage at a higher resonant frequency.

The quality factor of the on-chip inductance is the most important parameter that degrades the performance. So, careful layout design can result in substantial improvement [6]. For instance, connecting the inductor in a shunt configuration instead of in serial to the signal path can reduce the impact of substrate capacitance, and consequently reduce the losses.

B. RF to DC Rectifier

A basic schematic of a Villard voltage doubler, sometimes also called Cockcroft-Walton voltage multiplier, is shown in Fig. 4 (a). A DC voltage of twice the peak amplitude of the input AC signal can be generated at the DC output. And ideally, arbitrary output DC voltage can be reached by building cascaded stages of the doubler, Fig. 4 (b).

In the real case, the amplitude of the AC signal will be divided by coupling capacitors and the junction capacitance of the diode. Also the reverse leakage current of the diode and the resistance of the diode will limit the feasible DC output. Therefore, to obtain the maximum voltage, large coupling and charge-storage capacitance is preferred. In addition, larger capacitance stores more energy and consequently provides more current when discharging. Low series resistance Schottky diodes are most suitable for implementing the circuit due to its high forward bias current for a given voltage. According to the analysis above, the junction capacitance should be minimized to achieve higher output voltage.

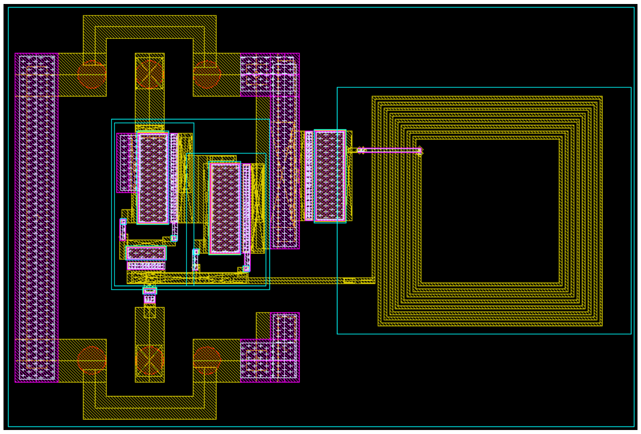

Fig. 5. Layout of the testing circuit, including the boosting network and the rectifier circuit

By coupling the AC signal to the diodes through capacitors in parallel instead of in series, a Dickson [7] voltage multiplier, as shown in Fig. 4 (c)-(d), provides stronger current drive ability with the penalty that the capacitors have to withstand the full DC voltage developed along the chain. A comparison of the two rectifier topologies is made. As the simulation results show in Section III, the two topologies reveal no significant difference at the voltage level of our interest.

The equivalent input impedance of both two rectifiers is decided by the diode junction capacitance, which is much smaller than the serially connected coupling and storage capacitance. When connect the rectifier to the boosting network, the equivalent capacitive load will decrease the resonant frequency and reduce he voltage boosting ratio. Therefore, careful component values have to be selected.

III. IMPLEMENTATION AND SIMULATION RESULTS

The circuit is implemented in a Silicon-on-Glass substrate transfer technology [8]. Using laser-annealed back-wafer contacts and thick copper metal layer, the technology provides high-performance low-loss Schottky diodes and on chip passives.

The testing circuits consist of a boosting network and followed by a two-stage voltage doubler rectifier. One circuit uses Villard doubler, while the other employs Dickson multiplier. Both circuits are optimized at 868.3 MHz for maximum output DC voltage, when a -20dBm RF signal is provided.

The layout of the testing circuit using Villard voltage doubler is shown in Fig. 5. The chip size is 1μm by 2 μm. As discussed in Section II, a large size inductor is designed to maximize

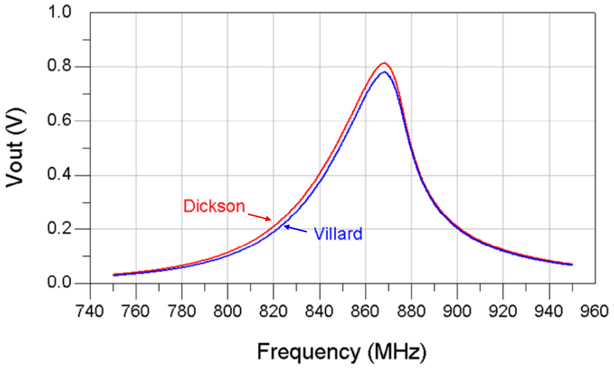

Fig. 6. The output DC voltage as a function of input signal frequency, with -20 dBm signal power and open circuit load.

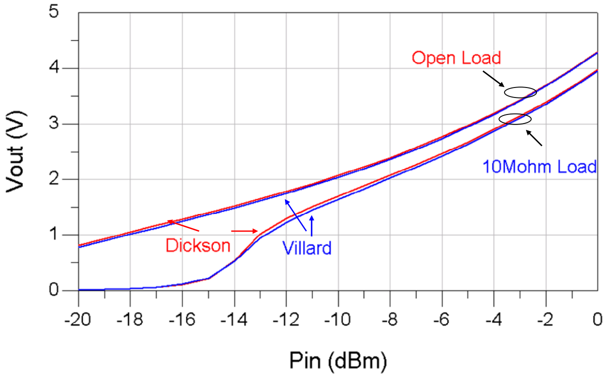

Fig. 7. The out put DC voltage as a function of input signal power, at 868.3 MHz and for both open circuit load and 10Mohm load.

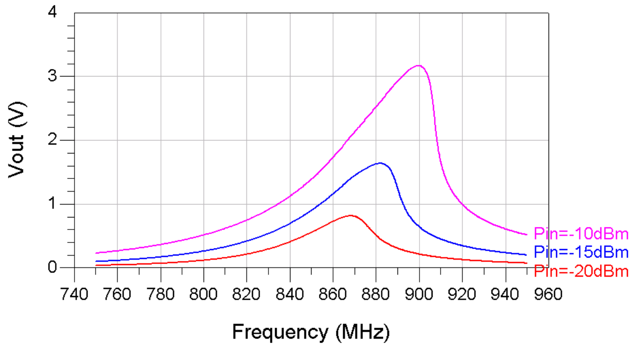

Fig. 8. The out put DC voltage as a function of input signal frequency, for different input signal power and open circuit load.

output voltage. And small Schottky diode size is used to minimize the junction capacitance.

An ADS simulation that takes into account the losses caused by component resistance and parasitics was performed. Fig. 6 shows the simulation result of output DC voltage as a function of the input RF signal frequency. When the load is an open circuit, 0.8V DC can be achieved when available antenna power is -20dBm. Again, Villard voltage topology and Dickson topology reveal no significant difference.

Fig. 7 shows the generated voltage in corresponding to input signal power at 868.3 MHz. In fact, when the received signal strength increases, the highest voltage output is achieved at a higher frequency. This is because the increase of reverse voltage on the diode results in a lower junction capacitance, which consequently leads to a higher resonant frequency. This is shown in Fig. 8.

The output voltage is independent on the charge storage capacitance. Larger capacitance stores more energy, and only takes longer charging time. More rectifier stages can be cascaded to achieve higher voltage. However, stages more than 5 will not bring substantial improvement for the power levels considered, due to energy losses along the chain.

IV. CONCLUSION AND FUTURE WORK

In this paper, we presented the design considerations of an integration scheme of RF energy harvesting. In this scheme, a resonant tank is used to achieve sufficient voltage swing required to drive the following rectifier stage. The rectifier converts RF power into DC energy as stored charge in the capacitors. Simulation results showed that the proposed scheme was a promising solution for long distance self-power wireless application.

Measurement of the circuits will be done once the fabrication completes. The use of dedicated antenna might be able to replace the resonant tank, which also will be studied in the future. The complete integration of the energy harvesting circuit block with ultra low power RFID circuitry will be the focus of future research.

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His research interests include RFID, ultra-low-power RF, and unobtrusive radio.